

2SK222

N-Channel Junction Silicon FET

Low-Noise AF Amp Applications

FEATURES

- Ultra low noise figure
- Large $|y_{fs}|$
- Low gate leakage current.

ABSOLUTE MAXIMUM RATINGS/ $T_a = 25^\circ\text{C}$

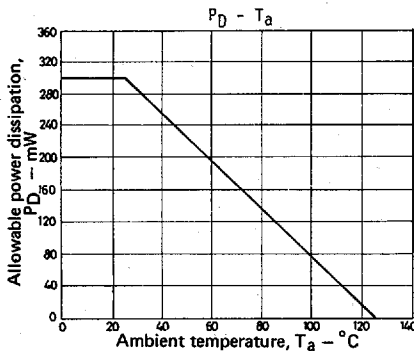
			unit
Drain-source voltage	V_{DS}	40	V
Gate-drain voltage	V_{GDS}	-40	V
Gate current	I_G	10	mA
Allowable power dissipation	P_D	300	mW
Junction temperature	T_j	125	$^\circ\text{C}$
Storage ambient temperature	T_{stg}	-40 to +125	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS/ $T_a = 25^\circ\text{C}$

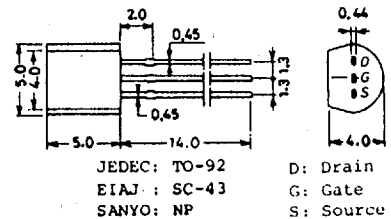
			min	typ	max	unit
Gate-drain breakdown voltage	$V_{(BR) GDS}$	$I_G = -100 \mu\text{A}$	-40			V
Gate cut-off current	V_{GSS}	$V_{GS} = -20 \text{ V}$			-1.0	nA
Cut-off voltage	$V_{GS} \text{ (off)}$	$V_{DS} = 10 \text{ V}, I_D = 10 \mu\text{A}$		0.5		V
Drain current	I_{DSS}	$V_{DS} = 10 \text{ V}, V_{GS} = 0$	0.6*		12.0*	mA
Forward transfer admittance	$ y_{fs} $	$V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1 \text{ kHz}$		17		mS
Input capacitance	C_{iss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$		14		pF
Feedback capacitance	C_{rss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$		3.5		pF
Noise figure	NF (1)	$V_{DS} = 10 \text{ V}, V_{GS} = 0, R_g = 1 \text{ k}\Omega, f = 100 \text{ Hz}$		1.0	3.0	dB
	NF (2)	$V_{DS} = 10 \text{ V}, V_{GS} = 0, R_g = 1 \text{ k}\Omega, f = 1 \text{ kHz}$		0.6	1.5	dB
Equivalent input noise voltage	V_{NI}	$V_{DS} = 10 \text{ V}, V_{GS} = 0, R_g = 1 \text{ k}\Omega, f = 1 \text{ kHz}$		2		$\text{nV}/\sqrt{\text{Hz}}$

* 2SK222 is graded as follows by drain current I_{DSS} (unit : mA).

0.6 C	1.5	1.2 D	3.0	2.5 E	6.0	5.0 F	12.0
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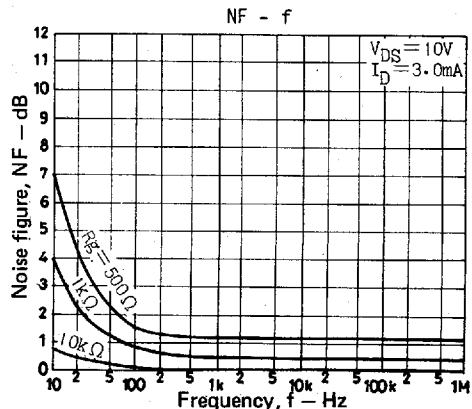
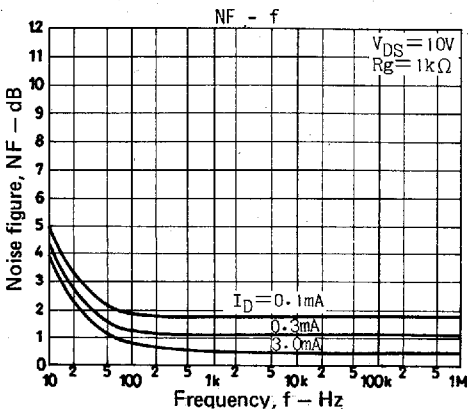
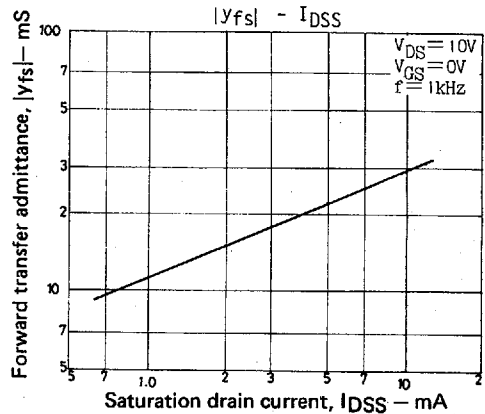
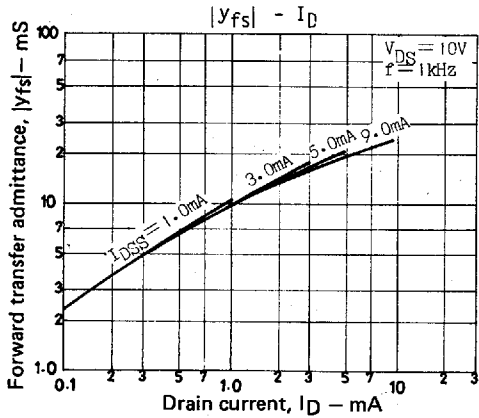
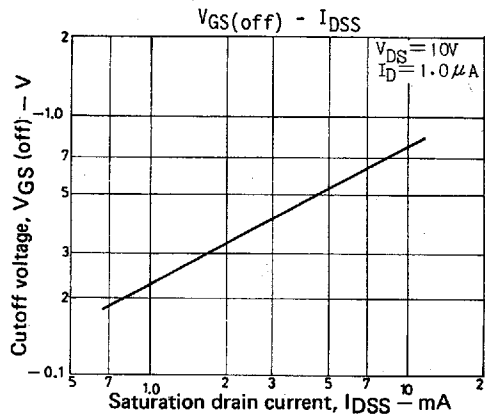
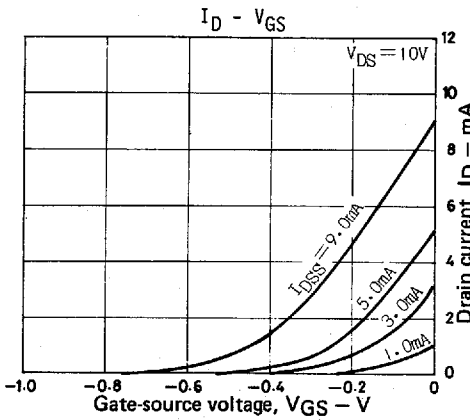
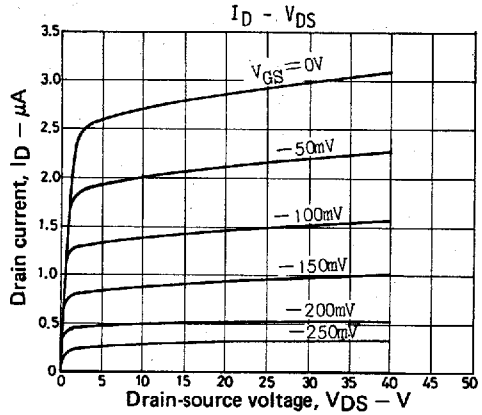
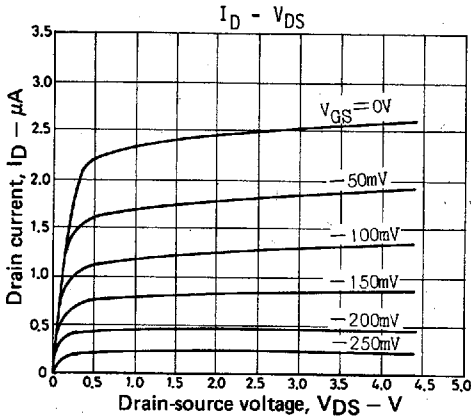
Case Outline 2019A (unit : mm)



Specifications and information herein are subject to change without notice.

SANYO Electric Co., Ltd. Semiconductor Business Headquarters

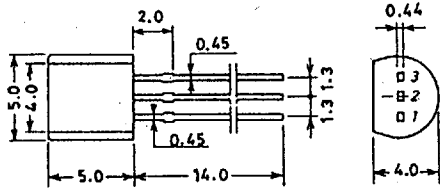
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN



CASE OUTLINES OF LEAD FORMED SMALL SIGNAL TRANSISTORS

- All of Sanyo lead formed small signal transistor case outlines are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.
- No marking is indicated.

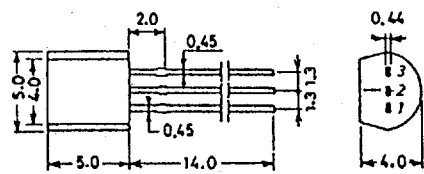
Case Outline 2003A/2003B (unit : mm)



JEDEC : TO-92
EIAJ : SC-43
SANYO : NP

1 : Emitter
2 : Collector
3 : Base

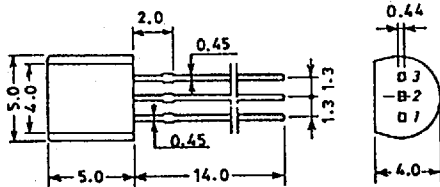
Case Outline 2019A/2019B (unit : mm)



JEDEC : TO-92
EIAJ : SC-43
SANYO : NP

1 : Source
2 : Gate
3 : Drain

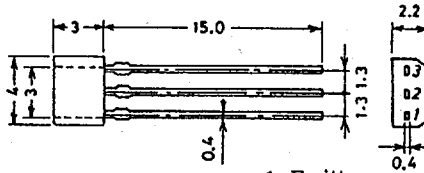
Case Outline 2004A (unit : mm)



JEDEC : TO-92
EIAJ : SC-43
SANYO : NP

1 : Base
2 : Emitter
3 : Collector

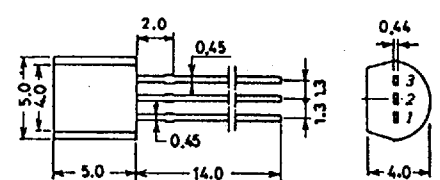
Case Outline 2033 (unit : mm)



1 : Emitter
2 : Collector
3 : Base

SANYO : SPA

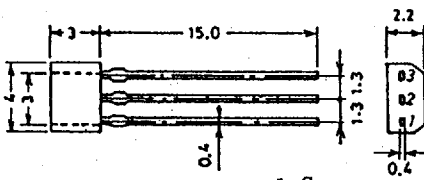
Case Outline 2005A (unit : mm)



JEDEC : TO-92
EIAJ : SC-43
SANYO : NP

1 : Drain
2 : Source
3 : Gate

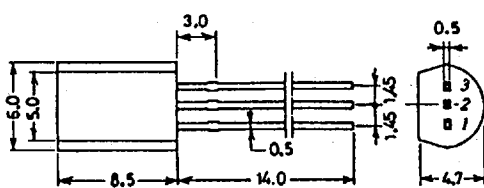
Case Outline 2034/2034A (unit : mm)



1 : Source
2 : Gate
3 : Drain

SANYO : SPA

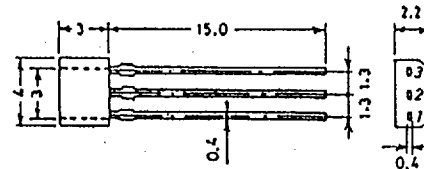
Case Outline 2006A (unit : mm)



EIAJ : SC-51
SANYO : MP

1 : Emitter
2 : Collector
3 : Base

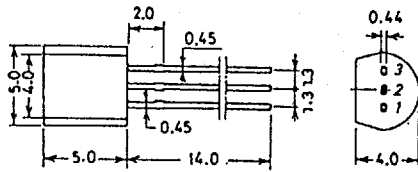
Case Outline 2040 (unit : mm)



1 : Drain
2 : Source
3 : Gate

SANYO : SPA

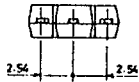
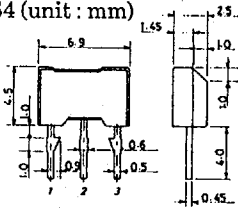
Case Outline 2061 (unit : mm)



JEDEC : TO-92
EIAJ : SC-43
SANYO : NP

1 : Emitter
2 : Base
3 : Collector

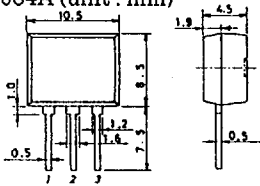
Case Outline 2064 (unit : mm)



1 : Emitter
2 : Collector
3 : Base

SANYO : NMP

Case Outline 2084A (unit : mm)



1 : Emitter
2 : Collector
3 : Base

SANYO : FLP